REMARKS

The Examiner rejected claims 1-6 under 35 U.S.C. 103(a) as being unpatentable over Kumar *et al* (hereafter "Kumar")(US 2003/007 6899) in view of Kodama *et al* (hereafter "Kodama") (US 7,023,324). Applicant submits that claims 1, 2, 4, and 6 as currently amended are not obvious in view of the cited prior art. Applicant traverses the rejection of claims 3 and 5.

First, claim 1 has been amended to make it clear that in any given input polyphase cycle, at least one of the filters processes a plurality of different polyphase components stored in the memory from a corresponding polyphase cycle.

The Examiner identifies the outputs of the ADCs 36a---36m as a plurality of polyphase components. Applicant submits that Kumar teaches (paragraph 0044) that "The first sampled signal output at the sampler 34a output is digitized by the analog-to-digital converter 36a which produces at its output the first digital signal", "The second sampled signal is input to an analog-to-digital converter 36b, which creates the second digital signal at its output" and so on. Hence, Applicant submits that Kumar teaches that, at most, a **single** digital signal is stored in the output buffer of each ADC prior to being sent into the following filter. Accordingly, Applicant submits that each filter in the system taught by Kumar processes only a single polyphase component stored in the "memory" identified by the Examiner from a corresponding polyphase cycle.

Hence, Applicant submits that neither Kumar nor Kodama teach the limitation of claim 1 requiring each filter to process a plurality of different polyphase components stored in the memory from a corresponding polyphase cycle.

Second, the Examiner states that Kumar does not teach a multiplexer that outputs the filtered polyphase components in a predetermined order to generate a filtered output signal. The Examiner looks to Kodama for the missing teachings. The Examiner maintains that it would have been obvious to implement the teaching of Kodama into Kumar "to select the sub-carrier in such a manner that the frequency position where the large noise component

would be present may be previously avoided so that the communication having higher reliability could be realized as taught by Kodama (col. 21, lines 37-40)".

Applicant submits that there would be no expectation of success in applying the multiplexer of Kodama to the system of Kumar as suggested by the Examiner, as the multiplexer would reduce the throughput of the system taught by Kumar rather than convey a benefit.

First, the Examiner suggests that the multiplexer mentioned by Kodama would be placed at the output of the filters in Kumar. In this configuration, the output of the filters in Kumar would be read out in serial order into the FFT generator 18. The FFT generator could not proceed until the filter outputs, or a substantial fraction of them, were received. Hence, there would be a delay between the generation of the filtered values and the start of the FFT. In contrast, Kumar already teaches a system that lacks this delay. Hence, there must be some advantage in making the alteration in Kumar to overcome the disadvantage of including another hardware element and a delay in the processing. Since the FFT processor operates on the same filter values, the result of the FFT must be the same. Hence, the output of the FFT could not provide any function that the original FFT output could not have provided. Accordingly, there is no reasonable expectation of success in making the modifications suggested by the Examiner.

It should also be noted that Kodama teaches (column 21, lines 8-41) that the benefit of higher reliability by sub-carrier frequency selection suggested by the Examiner is the result of a noise level filtering operation carried out by elements 115 and 116 in embodiment mode 11 not the inclusion of a multiplexer. The Examiner has not pointed to any teaching that the upsamplers 302, adders 303, and delay elements 304 identified (column 17, lines 29-34) as equivalent to a multiplexer in embodment mode 9 are involved to any extent at all in this noise filtering operation.

Accordingly, Applicant submits that the Examiner has failed to make a *prima facie* case for obviousness with respect to claim 1 and the claims dependent therefrom.

Claim 3 requires that the memory comprises a shift register. The Examiner states that Kumar teaches a buffer (paragraph 0048) which the Examiner identifies as the memory recited in Claim 1. The Examiner maintains that it would be obvious to implement a shift register for this memory "to hold the binary word representing the sampled value for the time duration".

Applicant must disagree with the Examiner's reading of the cited passage. The memory identified by the Examiner is described simply as a buffer at the output of the analog-to-digital converter that holds the binary word output of the analog-to-digital converter prior to the output being shifted into the corresponding polyphase filter. There is no need for the buffer to be a shift register in order to hold a binary word representing the sampled value for a time duration as suggested by the Examiner. Since the cost of a shift register is substantially higher than that of a conventional buffer, nothing would be gained by using a shift register for the output buffer in the ADCs. Accordingly, Applicant submits that the Examiner has failed to make a *prima facie* case for obviousness with respect to Claim 3.

Claim 5 requires that the filters generate a filtered polyphase component that depends on a non-linear combination of the polyphase components. The Examiner points to Kumar paragraph [0033] as teaching this limitation. Applicant must disagree with the Examiner's reading of Kumar. First, the cited paragraph discusses a prior art system, not the invention of Kumar. Second, Applicant can find no mention of any non-linear transformation in the cited paragraph or anywhere else in Kumar. The passage mentions Hilbert transforms, but such transforms are well known to be linear transformations. Third, the system that is taught in Kumar performs a Fourier transform on the polyphase components. A Fourier transform is also well known to be a linear transformation.

Hence, Applicant submits that the Examiner has failed to make a *prima facie* case for obviousness with respect to Claim 5.

Respectfully Submitted,

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